

A Real-time Embedded FPGA Processor for a Stand-alone Dual-Mode Assistive Device

Ali Jafari¹, Maysam Ghovanloo², and Tinoosh Mohsenin¹

¹Department of Computer Science & Electrical Engineering, University of Maryland, Baltimore County

²School of Electrical & Computer Engineering, Georgia Institute of Technology

I. INTRODUCTION

Assistive Technologies (ATs) can help people with disabilities to perform many daily activities with minimal or no assistance and increase their independence. Multi-modal assistive devices can increase the number of alternatives available to users to perform different tasks simultaneously while giving users the ability to switch among different input sensor modalities, based on their needs, convenience, and environmental conditions. To convert the output of each sensor modality to a meaningful command, different signal processing stages, such as filtering, feature extraction and machine learning classification are needed to be performed. Usually, these are done on a cloud computer which requires the raw data to be sent. Transmitting raw data generated from different sensors to a PC/Smartphone for further signal processing results in high power consumption, which is not desired in battery-powered wearable assistive devices [1], [2].

This paper presents a stand-alone Dual-mode Tongue Drive System (sdTDS) which is designed for people with severe disabilities to control their environment using their tongue motion and speech. The sdTDS detects user's tongue motion using a magnetic tracer placed on tongue and an array of magnetic sensors embedded in a wireless headset and at the same time it can capture the user's voice using a small microphone embedded in the same headset. A real-time FPGA-based local processor is proposed which can perform all required signal processing at sensor side, rather than sending all raw data out to a PC or smartphone. The proposed sdTDS significantly reduces the transmitter power consumption and subsequently increases the battery life. The detected commands can be used for example for controlling a mouse and a wheelchair.

II. ALGORITHM DESIGN AND ANALYSIS

A. Tongue Drive

Tongue is an ideal candidate for developing a wearable AT device, because of fast movement with many degrees of freedom and high flexibility. TDS detects the tongue motion by measuring the magnetic field variation generated by a magnetic tracer glued to the user's tongue, using an array of magnetic sensors placed on a wireless headset. TDS mainly contains an external magnetic interference (EMI) attenuation and a machine learning (ML) classifier module. EMI attenuation module receives the data coming from 4 magnetometers and generates some features that can be used for classifying the user-defined commands. Multinomial Logistic Regression (LR) is used as the ML classifier.

B. Speech Recognition

Speech Recognition (SR) technology can produce literally unlimited number of available commands. The people with severe disabilities can take advantage of this technology as long as they have the ability to speak. A fast embedded SR design is proposed which can recognize different voice commands right at the microphone side, rather than sending all voice signals to a PC and using a SR software packages to process them. One way of recognizing a voice signal is to compare similarity of a signal to other pre-labeled voice signals. In this work, Cross-correlation algorithm is proposed to find the similarity of voice signals. The cross-correlation function is used to measure the similarity of two signals as a function of the displacement of one relative to the other. Any vector of input test voice signal is cross correlated by all training data. The training data include pre-labeled voice signals. The results of cross correlation of the input test signal with all the training data are compared to find a maximum. The label of that particular cross correlation which leads to a maximum, will be the label for the input test signal.

III. FPGA IMPLEMENTATION RESULTS

The complete proposed sdTDS solution which includes TDS and SR kernels is implemented on a Xilinx Zynq SoC device (ARM+Artix FPGA). The static power consumption of FPGA fabric is around 173 mW and the total power consumption of the design is around 677mW. The latency for TDS and SR to finish all computations for one window of input data is 6.6 μ S and 3.1 mS, respectively. Table I shows the device utilization breakdown of the proposed sdTDS on the Zynq processor.

TABLE I. sdTDS PROCESSOR RESOURCE UTILIZATION ON ZYNQ SoC DEVICE

Resource Utilization Summary			
Resource	Used (#)	Available (#)	Utilization (%)
DSP Slices	96	200	44
BRAM	16.5	140	12
Slice	8685	13300	65
Slice LUT	27544	53200	52
Slice Registers	27544	106400	31

REFERENCES

- [1] A. Jafari *et al.*, "A low power seizure detection processor based on direct use of compressively-sensed data and employing a deterministic random matrix," in *Biomedical Circuits and Systems Conference (BioCAS)*. IEEE, 2015, pp. 1–4.
- [2] A. Page, A. Jafari, C. Shea, and T. Mohsenin, "Sparcnet: A hardware accelerator for efficient deployment of sparse convolutional networks," *Journal on Emerging Technologies in Computing (JETC)*.