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CS-based Secured Big Data Processing on FPGA

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***Abstract*—The four V's in Big data sets, Volume, Velocity, Variety, and Veracity, provides challenges in many different aspects of real-time systems. Out of these areas securing big data sets, reduction in processing time and communication bandwidth are of utmost importance. In this paper we adopt Compressive Sensing (CS) based framework to address all three issues. We implement compressive Sensing using Deterministic Random Matrix (DRM) on Artix-7 FPGA, and CS reconstruction using Orthogonal Matching Pursuit (OMP) algorithm on Virtex-7 FPGA. The results show that our implementations for CS sampling and reconstruction are 183× and 2.7× respectively faster when compared to previously published work. We also perform case study of two different applications i.e. multi-channel Seizure Detection and Image processing to demonstrate the efficiency of our proposed CS-based framework. CS-based framework allows us to reduce communication transfers up to 75% while achieving satisfactory range of quality. The results show that our proposed framework is 290× faster and has 7.9× less resource utilization as compared to previously published AES based encryption.**

As the usage of Big Data sets is increasing, many industries such as banks, defense, and medical are worried about the security of Big information [1]. CS is a novel technique in which compression of the data set is performed by obtaining fewer linear combinations of data. CS randomizes the data set yielding a smaller encoded solution that cannot be recovered without the measurement matrix set. We propose a CS-based secured big data processing framework as shown in Figure 1. CS is adopted to reduce communication bandwidth while achieving secured communication transfers. Data is assembled in sparse measurements that can be used to secure streaming data or external memory data transfers to the processing platform. The framework has three important kernel 1. Compressive Sensing 2. CS Reconstruction [2] and 3. Measurement Matrix. In this paper, we implemented CS using DRM technique which acts as an "encryption" on the Artix-7 FPGA. Reconstruction of the sampled signal is achieved using the OMP algorithm which acts as "decryption" on the Virtex-7 FPGA. The Measurement Matrix is stored on chip in the FPGA cache and acts as the "Keys" to sampled signal. This platform assumes the FPGA is trustworthy and after reconstructing the signal the remaining resources on the FPGA can be used for Big Data processing.

References

[1] A. Kulkarni et. al. Real-Time Anomaly Detection Framework for Many-Core Router through Machine Learning Techniques. *ACM Journal on Emerging Technologies in Computing (JETC)*, 2016.

[2] A. Kulkarni et. al. Sketching-based high-performance biomedical big data processing accelerator. In *Circuits and Systems (ISCAS), 2016 IEEE International Symposium on*, 2016.

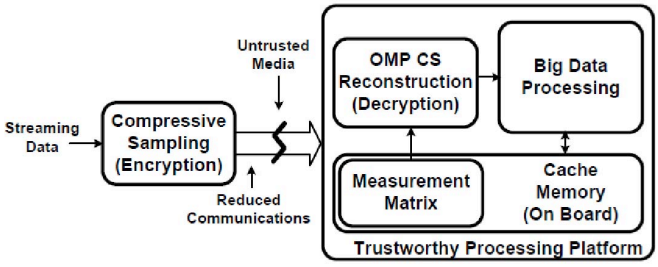

Fig. 1: Proposed CS-based Secured Big Data Processing Framework, where the Compressive Sensing kernel acts as an encryption in addition to reducing data, OMP CS Reconstruction kernel acts as an decryption and reconstruction of data, measurement matrix as keys

TABLE I: Case Study: Seizure Detection

EEG signal size: one second window (256 samples)		
Sampling (DRM)	Dynamic Energy(nJ)	10.62
	Execution Time (μS)	1.28
Reconstruction (OMP)	Dynamic Energy(μJ)	1.36
	Execution Time (μS)	10.12

TABLE II: Case Study: Image reconstruction Application

Image Size	128 × 128 32KB	256 × 256 64KB	512 × 512 128KB	1024 × 1024 256KB
CS Sensing using Deterministic Random Matrix (Artix-7)				
Dynamic Energy(μJ)	0.67	2.71	12.2	50
Execution Time (mS)	0.081	0.32	1.31	5.2
CS Reconstruction: OMP Algorithm (Virtex-7)				
Dynamic Energy (mJ)	0.08	0.39	1.4	11.5
Execution Time (ms)	1.3	2.9	6.82	49.15

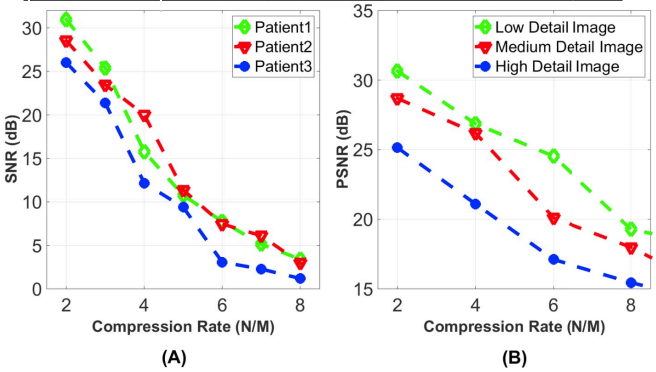

Fig. 2: (A) SNR vs Compression Rate for EEG data (B) PSNR vs Compression Rate for Image Data

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